Please revise the Attorney Docket No. from "P00,0253" to --09792909-0307--.

IN THE SPECIFICATION

Please substitute the paragraph beginning on page 1, line 2 with the following paragraph:

To increase the capacitance, Japanese Published Unexamined Patent Application No. Hei 8-306646 proposes a method in which hemispherical grained silicon (referred to as HSG-Si hereinafter) is formed on the surface of an electrode.

Please substitute the last paragraph on page 3 with the following paragraph:

In detail, organic substance that is generated during the process is deposited on the surface of the core pattern 2a formed on the cylinder core layer 2 described with reference to FIG. 3A. Such organic substance is taken into the core, pattern 2a side surface layer of the amorphous silicon film 3 formed so as to cover the inside wall of the core pattern 2a. A natural oxide layer that has grown on the surfact of the bottom electrode 3a is removed by means of etching of the bottom electrode 3a with diluted hydrofluoric acid, but amorphous silicon that is the component of the bottom electrode 3a and organic substance can not be removed by means of etching with diluted hydrofluoric acid. As a result, the surface layer of the bottom electrode 3a where organic substance has been taken in remains.

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Please substitute the first paragraph on page 9 with the following paragraph:

Next, the inter-layer insulating film 13 is subjected to anisotropic etching with aid of a resist patter used as a mask not show in the drawing to thereby form a contact hole 14 that

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extends to the semiconductor substrate 11 on the inter-layer insulating film 13. Herein, a diffusion layer formed on the semiconductor substrate 11 just under the contact hole is not shown in the drawing. Then, the resist pattern is removed, and a conductive layer is embedded in the internal of the contact hole 14 to obtain a contact electrode 15 that is connected to the semiconductor substrate 11. Next, an etching stopper layer 16 is formed on the inter-layer insulating film 13 and the contact electrode 15. The etching stopper layer 16 is a layer having a film thickness of, for example, 100nm consisting of silicon nitride to be served as a stopper layer when a cylinder core layer is removed later.

Please substitute the paragraph beginning on page 11, line 12 with the following paragraph:

The amorphous silicon film 18 disposed on the cylinder core layer 17 is removed by means of CMP process in the above-mentioned case, otherwise a method, in which a silicon oxide film (for example, NSG) is formed [is formed] on the amorphous silicon film 18 at a temperature that is not favorable for crystallization of amorphous silicon. The silicon oxide film and amorphous silicon film 18 are removed by means of isotropic RIE (reactive ion etching) process from the surface side of the silicon oxide film to thereby remove partially the amorphous silicon film 18 excepting the amorphous silicon film 18 that covers the inside wall of the core pattern 17a.

Please substitute the paragraph beginning on page 21, line 14 with the following paragraph:

Thereafter, as shown in FIG. 2G, a natural oxide film (not shown in the drawing) generated on the surface layer of the bottom electrode 39a and the exposed amorphous silicon surface layer that is the component of the bottom electrode 39a are removed by means of etching. Herein, the natural oxide layer (not shown in the drawing) and the exposed amorphous silicon surface layer that is the component of the bottom electrode 39a are removed by means of etching with a strong alkaline aqueous solution etchant. The wet etching is carried out in the same manner as used in the first embodiment described with referenced to FIGF.1F.

IN THE CLAIMS

Please cancel claim 2.

Please amend claims 1 and 4 as follows.

1. (Amended) A method for forming a capacitor comprising:

a first step for forming an amorphous silicon film so as to cover hole-type or island-type core pattern formed on a substrate,

a second step for removing said amorphous silicon film so that said amorphous silicon film remains on the side wall of said core pattern to thereby form a cylindrical bottom electrode having the peripheral wall that is said amorphous silicon film remaining on the side wall of said core pattern,

a third step for removing said core pattern by means of etching,